Session - 3

Memory and I/O Interfacing - I

Session Objectives

At the end of this session, the learner will be able to:

- Understand the memory devices and their characteristics.
- Identify the interconnection of a memory element to a CPU.
- Illustrate the differences in speed of CPU and memory.
- Know about the Wait state and their applications.
- Compare the Read and Write operation of memory and I/O devices.

Teaching Learning Material

- Board
- Presentations
- Manufacturer's Data sheets
- Laboratory Manual

Session Plan

Time (in min)	Content	Learning Aid / Methodology	Faculty Approach	Typical Student Activity	Skill/Competency Developed
10	Introduction	Board React to Situation Activity	Explains Facilitates	Listens Participates	Knowledge Comprehension Intrapersonal
15	Types of Memory	Board Chart Presentation Associate Activity	Explains Facilitates	Listens Participates	Knowledge Comprehension Analysis Interpersonal Intrapersonal Kinematics
15	Interfacing Microprocessor with memory	Board Presentation	Explains Facilitates	Listens Participates	Knowledge Comprehension Analysis Intrapersonal
10	Memory Timing Requirements	Board Presentation	Explains Facilitates	Listens Participates	Knowledge Comprehension Analysis Intrapersonal
10	Conclusion and Summary	Team Quiz Activity Discussion	Explains Facilitates	Participates Analyzes Answers	Knowledge Comprehension Analysis Application Interpersonal Intrapersonal

Session Inputs

Introduction

In the previous session we discussed about the way a device communicates with the CPU. The timing diagrams we drew provided an insight to the compatibilities between CPU and Memory or I/O devices. We also drew the timing diagram with the assumption that memory and the CPU speeds were same.

In this session, we shall see how to connect memory and CPU that have varying speeds. Normally memory speeds are slower than that of the CPU speeds.

We shall start our session with an activity to understand the different memory speeds before discussing the various types of memory and their interfacing techniques.

Suggested Activity: React to Situation

Let us call 3 learners to react to a situation where each of them wants to make a telephone call to one of their friends whose phone number is not available with them at that instant. They also do not have their mobile handset with them to refer the phone number.

Typical Reactions could be:

1. They remember the phone number.
2. They had scribbled the number in a phone book which they would refer.
3. They will look into the telephone directory.

We could write down these reactions on the board and lead the discussion towards:

1. The first method helps recollect the phone number fastest, and it is not dependent on any other resource; but it has limited storage capacity and can be updated.

2. The second method is slower than the first one; but the storage capacity is more than the first method. It depends on a resource and can be updated.
3. The third method is the slowest and has maximum storage capacity. It depends on external resources and cannot be updated.

All the above three observations correspond to different types of memory that are used for diverse applications with varying storage capabilities. Each type of memory will have a different operating speed and is normally slower than the CPU speed. We need to ensure proper data transfer between the CPU and memory without any data loss.

Types of Memory

We can ask the learner's to list a few memory types. As the learner's give their answers we could capture them in a table along with their respective technology.

Type of Memory	Technology
RAM	Semiconductor
ROM /PROM/EPROM/EEPROM	Semiconductor
Hard disk	Magnetic
Floppy disk	Magnetic
Tapes	Magnetic
Flash memory	Volatile non volatile memory
CD R/W	optical

In this session, we will focus only on the semiconductor memory. We will start with Random Access Memory (RAM) and later move on to **Read Only Memory (ROM).**

Random Access Memory (RAM)

RAM can be ***Static*** or ***Dynamic***. A Static RAM (SRAM) cell uses a Flip-Flop to store a bit. A dynamic RAM (DRAM) cell uses a capacitor to store one bit.

Now we can ask the learner's to compare and contrast SRAM with DRAM. Tabulate the responses as shown.

Suggested Activity: Associate

Let us present on board the following properties of RAM. We can randomly call the learners to come to the board and associate the properties with the corresponding RAM type with the help of an arrow.

Properties
Requires minimum of two transistors per bit
Requires one transistor and a capacitor (capacitor can be two wires running parallel) per bit.
Retains the data as long as power is available
Has low storage capacity
Needs periodic refreshing, as the capacitor discharges from time to time.
Has high storage capacity

Type of RAM
DRAM
SRAM

Read Only Memory (ROM)

There are 3 types of ROMs:

- Programmable ROM (PROM)
- Erasable Programmable ROM (EPROM)
- Electrically Erasable Programmable ROM (EEPROM)

PROM: PROMs have fuses to store one bit. Passing a high current will burn the fuse and change the logic level. Once programmed, PROMs cannot be re programmed.

EPROM: EPROMs are similar to PROMs. But, we can erase (and hence reprogram the EPROM by exposing them to UV rays.

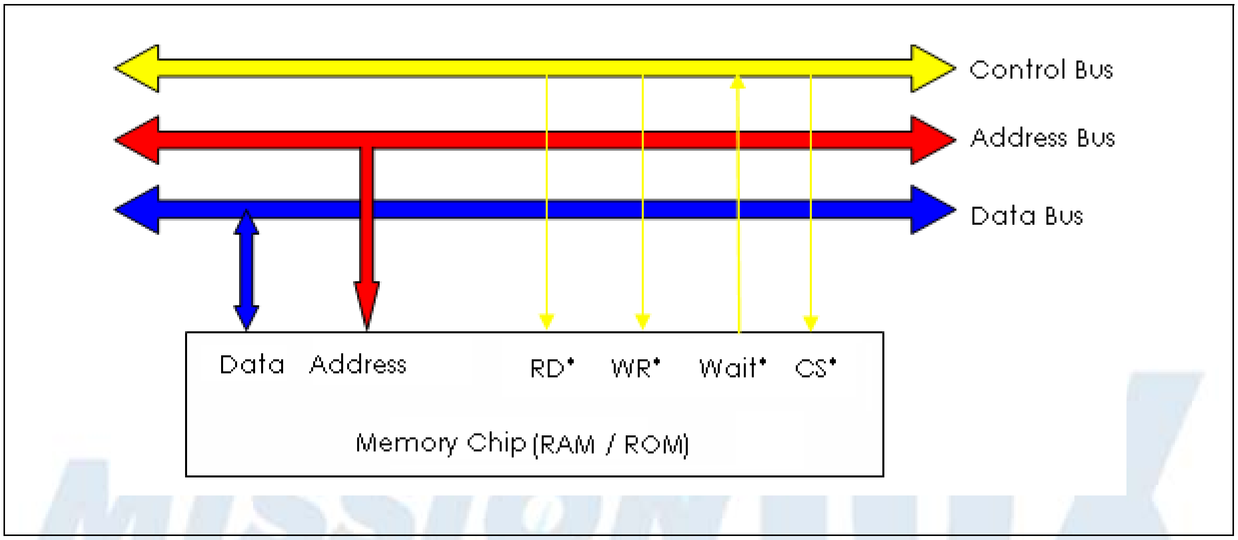
EEPROM: EEPROMs are similar to EPROMs. Here, data can be erased electrically instead of UV rays.

Let us now see how an SRAM or ROM can be interfaced with a Microprocessor.

Interfacing Microprocessor with Memory

Notes

We can draw a simple block diagram of interfacing memory (SRAM/ROM) to a CPU



Announcement

When the speed of memory and the CPU are comparable, we can connect the memory and CPU as shown above. We see that the data bus and address bus are connected directly to the memory chip.

We tap the Read signal (RD*) and the Write signal (WR*) from the control bus and connect it to the memory. The Chip Select (CS*) logic has to be generated. We will explain the CS* logic in the next session.

Connection diagram for SRAM and ROM will be same as shown above.

In this case, we mentioned that the speeds of memory and CPU are comparable. Now let us discuss how different speeds of memory and CPU can be interfaced. But before we do so, let us first re-cap the timing diagram from the previous session.

Memory Timing Requirements

We shall display the same timing diagram which we used for the previous session. Then let us ask the learner's to define:

- Access time
- Set-up time
- Latch-up time

We can also quiz the learner's on what would happen if the access time of a memory is more than the Read/Write time of a CPU?

For the connection diagram shown above with the control signals Wait* and CS* we can ask the learner's to draw the timing diagram.

While assisting the learner's to draw the diagram, we could also highlight the following:

- CS* signal is used to select the memory chip, either ROM or SRAM
- Wait state signal (WAIT*) would decide the time to wait between the Read or Write cycles, also highlight that this delay would extend to multiple clock cycles
- The CPU waits for an acknowledgement signal from the memory

With reference to the timing diagram provide the following details:

- In the 8085/8086 architectures, the memory (or some control circuitry) will introduce a wait state.
- The wait signal will be asserted during the T2 cycle.
- This will delay the de-assert phase of RD* or WR* in T3.
- The RD* or WR* will remain at logic low as long as READY* signal is low.
- If the READY* signal is de-asserted at Tn cycle, RD* or WR* will be de-asserted at Tn+1 cycle.
- This stretching of RD* or WR* signal should be sufficient for the slow memories to transfer the data to the faster CPU.
- Wait states can be introduced in multiples of clock cycles.
- CPU waits for an acknowledge signal from the memory, until this signal is not received, it keeps the RD* or WR* signal asserted.
- The Memory chip acknowledges the transaction completion.

Remember to update the learner's that the same timing diagram can be used for accessing a slow speed I/O device.

After explaining the above concepts in detail, we can conclude the session with an activity.

Conclusion

Suggested Activity: Team Quiz

Let us divide the learner's into two teams, all odd numbered learner's form the A team and the even numbered learner's the B team. Team A shall ask questions to Team B on Memory Interfacing and Team B shall ask questions on I/O Interfacing to Team A. Each team shall ask 10 questions alternatively and we could track the scores. Typical questions could include:

1. What signals are needed for reading and writing into a memory element?
2. Why do we need a wait state while interfacing a slow memory device to a faster CPU?
3. How does READY* signal help?
4. For the 8085 LXI instruction to get executed, data is read from the memory. How many clock cycles does it need to complete this operation?
5. In the above question what will happen if we insert one wait state?

Summary

In this session, we learnt to:

- Identify and classify various types of memory
  - RAM
    - SRAM
    - DRAM
  - ROM
    - PROM
    - EPROM
    - EEPROM
- Explain the effects of speed disparity between various circuit elements.
- Illustrate the flow sequence between memory and CPU with the help of a timing diagram.
- Extend timing diagram for 8085 and 8086.

Assignments

1. Identify memory chips / devices that are used in computers. Study the data sheet of these devices and identify the timing diagram for Read and Write cycles.

Notes